# A Wideband OOK Receiver for Wireless Capsule Endoscope

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**Abstract— An on-off keying (OOK) receiver for wireless capsule endoscope application is presented, which comprises low-noise amplifier (LNA), band-pass filter, envelope detector, automatic-gain control (AGC) and output buffer. The common-drain-feedback LNA provides wideband input matching. Moreover, a high-frequency envelope detector has been implemented, which is based on OTA-rectifier-peak-detector open loop structure. The storage capacitor of the envelope detector is optimized to obtain good sensitivity and high data rate. A discrete-step AGC is applied for wide input dynamic range, which adopts forward gain-control technique to enhance the settling speed. The carrier frequency is 480 MHz. Sensitivity of the proposed receiver is measured to be -83 dBm, -81 dBm and -80 dBm with data rates of 10 Mbps, 20 Mbps and 40 Mbps, respectively.**

## I. INTRODUCTION

Wireless capsule endoscope is a promising non-invasive medical procedure for gastro-intestine (GI) tract examination. The capsule is swallowed by a patient and traverses the entire GI tract while wirelessly transmitting images of the GI tract to external receivers worn by the patient [1]. To obtain accurate images, the receiver is required to achieve a wide input dynamic range. Especially, the data rate is essential for the endoscope to get high-quality images when it passes through gullet [2].

Since the OOK receiver has simple structure, it can be implemented with a small chip size. Traditional super-heterodyne OOK receiver incorporates LNA, mixer, PLL, IF filter, logarithmic amplifier (IF amplifier) and demodulator. Usually off-chip resistors and capacitors are necessary for the loop filter in the PLL. The OOK receiver in [3] uses envelope-detection technique to get rid of the frequency conversion circuits like the mixer and PLL, which improves integration and reduces power consumption. Based on this configuration, an OOK receiver is proposed for the wireless capsule endoscope system in this paper.

The receiver is designed with wide bandwidth to satisfy the requirement of high date rate. In the RF front-end, the LNA applies common drain feedback structure to achieve wideband input matching. Besides, a high-frequency envelope detector realizes envelope amplitude demodulation. The value of the storage capacitor in the envelop detector is critical. Large capacitance can reduce the ripple and improve the sensitivity. But it degrades the track speed and limits the data rate. In this paper, allowable range of the capacitance has been deduced according to the requirement of ripple and track speed. Most importantly, the way to relax the trade-off between sensitivity and data rate has been presented. At the baseband processing, a simple discrete-step AGC is adopted for the wide dynamic input range, which has forward-control network to improve the settling speed.

## II. RECEIVER ARCHITECTURE

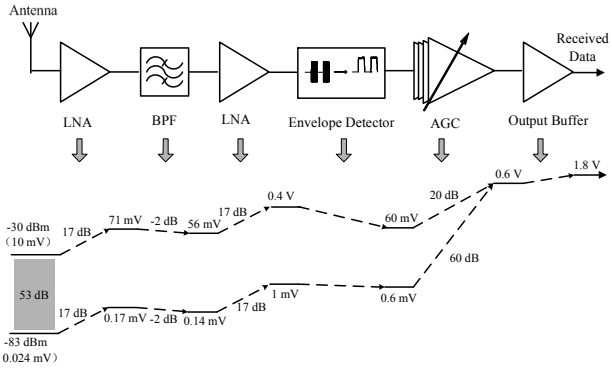


Fig. 1 OOK receiver architecture and power strength level flow

Fig.1 shows the proposed OOK receiver architecture and gain budget. The OOK modulated signal is received by the antenna and amplified by LNAs. A band-pass filter is inserted to suppress the spurious signals and strong out of band interferer. Then the envelope detector demodulates the base-band signal by directly extracting the amplitude information of the input signal. The AGC maintains the magnitude of the final output voltage constant against different receiving power. Here, AGC works at the base-band frequency of about several tens of MHz, therefore, its complexity is greatly reduced. Finally, the output buffer generates the digital signal for the following ASIC chip.

The signal strength level at various points of the receiver is denoted by voltage amplitude in Fig.1. The required sensitivity for the OOK receiver is -80 dBm for 40Mbps data transmission, but the design target is -83 dBm with 3-dB margin. For the 53-dB input dynamic range, the gain-distribution for each stage should be carefully designed to reduce the effects of noise and distortion. The signal-to-noise ratio (SNR) is a key for small signal. As the signal increases, the gain of the receiver should be reduced to prevent distortion.

After the LNA and band-pass filter stages, the input signal is amplified by 32 dB. Since the envelope detector in the paper is a weakly nonlinear circuit, which decreases the dynamic range to be 40 dB. In the baseband processing, the AGC provides the gain ranging from 20 dB to 60 dB with a 20-dB gain step. The output buffer enlarges the output signal to be the full-swing level (1.8 V).

## III. Circuit Implementation

### A. Low-Noise Amplifier

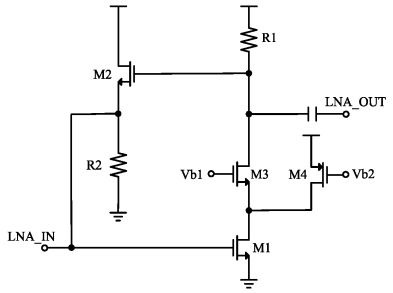


Fig. 2 Schematic of the single-ended LNA

The single-ended LNA in Fig.2 adopts the common-drain feedback consisting of M1-M3, R1 and R2 to achieve wideband input matching and high gain. Different from [4], the feedback network is DC coupled and the dc bias can be stabilized by itself, thus the chip size can be reduced. Besides, the transistor M4 provides the current-bleeding technique to relax the voltage headroom and enhance the transconductance of M1 [4].

### B. Envelope Detector

Fig.3 shows the schematic of envelop detector, which comprises a wideband OTA, a half-wave rectifier and a peak detector [5].

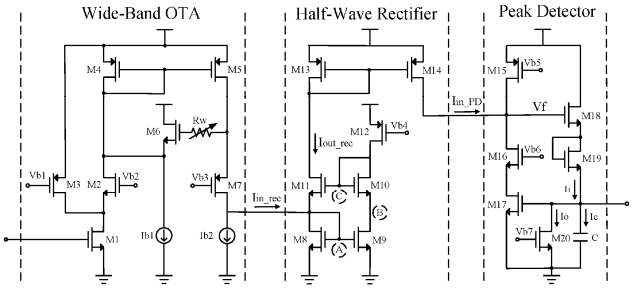


Fig. 3 Schematic of the proposed envelope detector

The OTA transforms voltage to current for the following rectifier. Since high transconductance of the OTA is desirable at RF stage to increase the sensitivity, the OTA adopts the current-bleeding technique constructed by M3. To expand the bandwidth, the OTA implements a gyrator-C active inductor consisting of M5, M6, M7, $R_w$, $I_{b1}$ and $I_{b2}$. Adopting high bias current in the rectifier can improve the operation speed of transistors and enhance the frequency performance. Therefore, transistors M8-M10 are biased in the saturation region instead of subthreshold region [5]. M11 initially in the subthreshold region acts as a current switch. As the current $I_{in\_rec}$ increases, the voltage at node A ($V_A$) increases and voltages at node B, C ($V_B$, $V_C$) significantly decrease. Then M11 is turned off and current $I_{out\_rec}$ falls to zero. When $I_{in\_rec}$ decreases, $V_B$, $V_C$ rise and $V_A$ drops, M11 turns on and $I_{out\_rec}$ increases. However, since the drain current of M8 reduces for the decreased $V_A$, $I_{out\_rec}$ will be smaller than $I_{in\_rec}$. Moreover, this current deviation is not linearly proportional to the amplitude of the input, which causes weak nonlinearity of the envelop detector.

The rectified current $I_{in\_PD}$ flows into the peak detector, which comprises a source follower M18-M20, a storage capacitor C, and a feedback path M16-M17. The current $I_c$ flowing through the capacitor is determined by the difference between input current $I_i$ and the bias current $I_0$. When $I_{in\_PD}$ increases, $I_c$ charges the capacitor and the output voltage quickly increases. Otherwise, if $I_{in\_PD}$ decreases, the input current $I_i$ is gradually reduced to zero, then $I_c$ becomes equal to the bias current $I_o$ discharging the capacitor. Because bias current $I_o$ is set to be very small, the output voltage will slowly respond to the decrease of the input signal. As a result, since charging current of the capacitor is much larger than the discharging current, the output voltage will track the peak value of input signal with only small ripple [6].

The peak detector has a trade-off between keeping and tracking operations. We can provide small descending slope of the output voltage to reduce ripple. However, this way increases tracking time for the data changing from 1 to 0 and limits the available data rate. Alternatively, a larger descending slope is used to improve the tracking capability, but it will generate larger ripple.

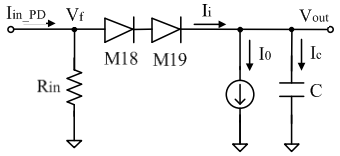


Fig. 4 Simple equivalent structure of peak detector

The peak detector can be simplified as the structure in Fig.4. Since M18 operates in the subthreshold region with the very small bias current $I_0$ and it can be modelled as a diode. $R_{in}$ represents the input impedance of the peak detector. Then the time constant $\tau$ can be given as [6]:

$$\tau = \frac{\zeta MC}{I_o} \tag{1}$$

where $\zeta$ =kT/q is a constant (25 mV) and M is the ideality factor of M18 and M19 in the subthreshold region. Based on the equation of the time constant, the descending slope of the output voltage can be expressed as:

$$\left(\frac{dV_{out}}{dt}\right)_f = \begin{cases} -\frac{1}{\tau}V_{out} = -\frac{I_o V_{out}}{\zeta MC}, & V_{out} \le \zeta M \quad (\text{case1}) \\ -\frac{I_o}{C}, & V_{out} > \zeta M \quad (\text{case2}) \end{cases} \tag{2}$$

The formula of the case 2 gives the maximum descending speed (slew rate). The ripple is critical for small signal. For the ripple to be lower than the noise for the minimum detectable signal, the upper limit of the ratio $I_o/C$ in (2) can be derived as follows.

$$\text{Ripple} \approx \frac{(dV_{out}/dt)_f}{2f_c} = \frac{I_o V_{out}}{2f_c \zeta MC} < V_{n,out} \Rightarrow \frac{I_o}{C} < \frac{2f_c \zeta M}{V_{out}/V_{n,out}} < \frac{2f_c \zeta M}{(SNR)_{\min}} \quad (3)$$

where $f_c$ is the carrier frequency. There is another consideration to determine the ratio $I_o/C$. Large signal causes long tracking time when the transmission data falls from 1 to 0. If the ratio of the tracking time over the period of one data bit should be smaller than λ, we can obtain the lower limit of $I_o/C$ using the formula (case 2) in (2):

$$(t_f)_{\max} = \frac{(V_{out})_{\max}}{(dV_{out}/dt)_f} = \frac{C(V_{out})_{\max}}{I_0} < \lambda \frac{1}{\beta} \Rightarrow \frac{I_o}{C} > \frac{\beta (V_{out})_{\max}}{\lambda} \quad (4)$$

where β represents the maximum data rate. Therefore, the above results give a design guideline to choose proper $I_o$ and C to satisfy the ripple level for a given data rate.

The diode-connected transistor M19 is in series with M18, which increases overall ideality factor M [7]. Fig.5 compares the simulated I-V characteristics in the log scale, which exhibits ideality factor M is 1.36 and 2.72 with M19 and without M19, respectively. Moreover, M19 can limit the maximum amplitude of output voltage $(V_{out})_{max}$. According to (3) and (4), we can see M19 enlarges allowable $I_o/C$ range and hence eases the compensation between the ripple and data rate.

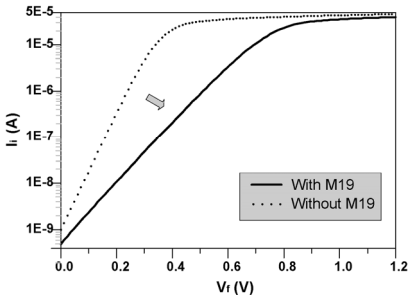


Fig. 5 I-V characteristics with and without M19, respectively

### C. Baseband Circuits

Fig.6 shows the structure of the AGC. The four-stage gain core is based on the simple common-source differential amplifier. The input buffer converts the single-ended signal from the envelop detector to the differential signal. The -3 dB bandwidth of the input buffer can be adjusted by the external capacitor Cb.

A1 is a fixed-gain amplifier. A2 and A3 are two variable-gain amplifiers. The gain-control networks of A2 and A3 are implemented by the series-connected resistor and NMOS switch transistor. When the control signal (Vc2, Vc3) is zero, the switching transistor is turned off and the variable amplifier exhibits similar operation as A1. When the control signal (Vc2, Vc3) is high, the switching transistor is turned on and the gain decreases. The FF1 and FF2 consist of a peak detector and a comparator, which check if the output amplitude of A1 and A2 are larger than the reference voltage Vref and controls Vc2 and Vc3, respectively. As the input signal of the receiver increases progressively from the minimum detectable signal level, AGC exhibits three cases in sequence: Vc2=Vc3=0; Vc2=0, Vc3=1 and Vc2=Vc3=1, which enables the two step gain control. Since the input resistance of the variable-gain stage decreases when the gain-control network is turned on, the load resistors of amplifiers are designed to increase stage by stage from A1 to A3.

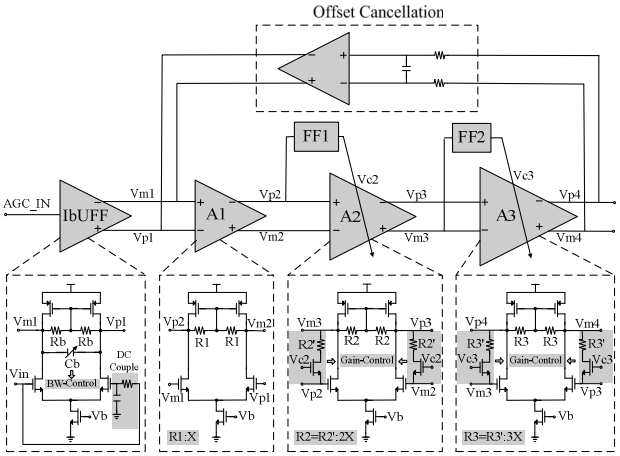


Fig. 6 Discrete-step AGC with offset cancellation

The output buffer including three inverters converts the output signal of the AGC to digital signal with full swing.

## IV. Experiment Results

The OOK receiver has been fabricated on TSMC 0.18-μm CMOS 1P6M process. This circuit dissipates 28.5 mA with a 1.8-V power supply. Fig.7 shows the chip microphotograph with an active area of 1.32 $mm^2$.

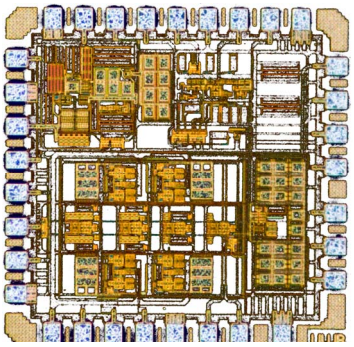

Fig. 7 Chip microphotograph of the OOK receiver

The off-chip band-pass filter in OOK receiver has the center frequency of 480 MHz and its bandwidth is 20 MHz. The OOK receiver is designed to achieve -80dBm input sensitivity with 40-Mbps maximum data rate. Therefore, the external storage capacitor C of the envelope detector in Fig.3 can be determined according to (3) and (4).

$$\frac{\beta (V_{out})_{\max}}{\lambda} < \frac{I_o}{C} < \frac{2f_c \zeta M}{(SNR)_{\min}} \Rightarrow 7.2\times10^6 < \frac{I_o}{C} < 16.32\times10^6 \quad (5)$$

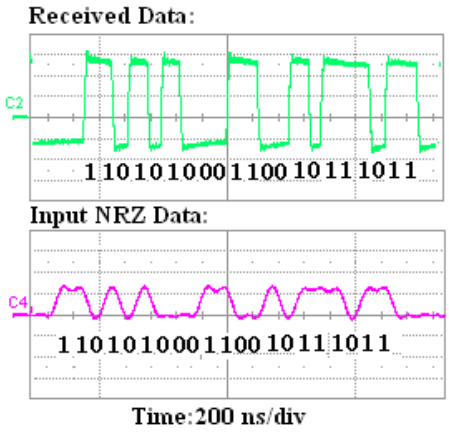


Fig. 8 Measured input and output waveforms for the data rate of 40 Mbps

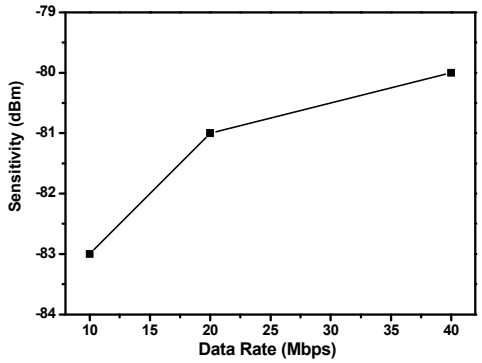


Fig.9 Measured sensitivity summary of the OOK receiver

TABLE I 1
PERFORMANCE SUMMARY OF THE OOK RECEIVER

| Performance | Measurement | | |
|---|---|---|---|
| Modulation | OOK | | |
| Carrier frequency | 480 MHz | | |
| Data rate | 10 Mbps | 20 Mbps | 40 Mbps |
| Sensitivity | -83 dBm | -81 dBm | -80 dBm |
| Power consumption | 28.5 mA | | |
| Chip size | 1.2 mm*1.1 mm | | |

In (5), 12-dB $(SNR)_{min}$ is used , which is the specification of OOK communication system to achieve $10^{-3}$ BER. We also assume $\lambda$= 1/3, which the ratio of the tracking time over the period of one data bit should be smaller than 1/3. The maximum output voltage of envelope detector $(V_{out})_{max}$ is about 60 mV. M and $\varphi$ are equal to 2.72 and 0.025, respectively. Carrier frequency fc is 480 MHz. $I_0$ is designed with 50 uA, then 3 pf <C<7 pf. Here, we select C=5 pf.

In the test bench, ESG signal generator produces 480 MHz carrier signal and downloads the none-return-to-zero (NRZ) 27-1 pseudo-random bit sequence (PRBS) data file from the computer, then generates the OOK modulation signal as the input for the receiver. Fig.8 gives measured input data and received data waveforms when the data rate is 40 Mbps. We can see the output signal exhibits the same pattern with the transmission data. Fig.9 summarizes the measured sensitivity of the OOK receiver, which is -83 dBm, -81 dBm and -80 dBm when date rate is 10 Mbps, 20 Mbps and 40 Mbps, respectively. Table 1 summarizes the detailed performance of the proposed OOK receiver.

## V. CONCLUSION

In the paper, we proposed an OOK receiver for the wireless capsule endoscope system. We have deduced the allowable range of the storage capacitor in the envelope detector according to the requirement of the ripple and tracking speed. Based on this analysis, the trade-off between sensitivity and data rate has been relaxed. For the baseband processing, a simple discrete-step AGC has been implemented with forward gain-control network to improve settling response. The proposed OOK receiver has been fabricated with TSMC 0.18-µm CMOS 1P6M process, which dissipates 28.5 mA current with a 1.8-V supply. Measurement results show that the OOK receiver achieved the sensitivity of -83 dBm, -81 dBm and -80 dBm when date rate is 10 Mbps, 20 Mbps and 40 Mbps, respectively.

## ACKNOWLEDGMENT

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